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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,714	07/15/2003	David J. Corisis	108298532US1	9586

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PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,714	CORISIS, DAVID J.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 January 0305*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62 and 64-83* is/are pending in the application.

4a) Of the above claim(s) *56,75 and 78-83* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *50 to 55, 57-59, 62, 64, 67-74, 76 and 77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/620714 Attorney's Docket #: 108298532US1
Filing Date: 7/15/2003;

Applicant: Corisis

Examiner: Alexander Williams

Applicant's Amendment filed 1/3/05 to the Applicant's election of species of figure 3 (claims 50-55, 57-74, 76 and 77), filed 6/29/04, has been acknowledged.

This application contains claims 56, 75 and 78-83 drawn to an invention non-elected without traverse in Paper No. 4.

Claims 1-49 and 63 have been canceled.

The disclosure is objected to because of the following informalities: The divisional application information should be updated with the patent information.

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 50 to 55, 57-59, 62, 64, 67-74, 76 and 77 are rejected under 35 U.S.C. 102(e) as being anticipated by Karnezos et al. (U.S. Patent Application Publication # 2004/0119152 A1).

50. Karnezos et al. (figures 1 to 18) specifically figure 2 show a packaged microelectronic devices **20**, comprising: a support member **12** having support member circuitry; a first packaged microelectronic device **(see 10 in figure 1A)** connected to at least one of the support member and the support member circuitry and having a first microelectronic die **14** generally encased **(by 17)** in a first encapsulant **17** to define a first package configuration; and a second packaged microelectronic device **(see 11 in figure 1B)** connected to at least one of the support member and the support member circuitry with the first packaged microelectronic device positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device having a second microelectronic die **24** generally encased **(by 27)** in a second encapsulant **27** to define a second package configuration different than the first package configuration, and wherein the second package microelectronic device is not fixedly attached to the first packaged microelectronic device.

51. The assembly of claim 50, Karnezos et al. further comprising a conductive connecting member **28** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to an outer edge of the first packaged microelectronic device.

52. The assembly of claim 50, Karnezos et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic

device extends outwardly beyond the second edge of the first packaged microelectronic device.

53. The assembly of claim 50, Karnezos et al. show wherein the first packaged microelectronic device has a first planform shape in a plane generally parallel to a plane of the support member and the second packaged microelectronic device has a second planform shape in a plane generally parallel to the plane of the support member, and further wherein the second planform shape is more extensive in at least one direction generally parallel to the plane of the support member than is the first planform shape.

54. The assembly of claim 50, , Karnezos et al. show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.

55. The assembly of claim 50, Karnezos et al. show wherein the second packaged microelectronic device has a plurality of conductive members **28** electrically coupled to the second microelectronic die and extending away from the second encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry without being attached to the first packaged microelectronic device.

57. Karnezos et al. (figures 1 to 18) specifically figure 2 show an assembly of packaged microelectronic devices, comprising: a support member **12**; a first packaged microelectronic device **(see 10 in figure 1A)** connected to the support member and having a first microelectronic die generally encased in a first encapsulant **17** to define a first planform shape; and a second packaged microelectronic device **(see 11 in figure 1B)** connected to the support member with the first packaged microelectronic device positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device having a second microelectronic die generally encased in a second encapsulant **27** to define a second planform shape different than the first planform shape.

58. The assembly of claim 57, Karnezos et al. show wherein the support member **12** defines a support member plane and the first planform shape describes an area in a first plane generally parallel to the support member plane that is smaller than an area described by the second planform shape in a second plane generally parallel to the support member plane.

59. The assembly of claim 57, Karnezos et al. further comprising a conductive connecting member **28** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.

60. The assembly of claim 57, Karnezos et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

61. The assembly of claim 57, Karnezos et al. show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.

62. The assembly of claim 57, Karnezos et al. show wherein the second packaged microelectronic device has a plurality of conductive members **28** electrically coupled to the microelectronic substrate and extending away from the second encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry.

65. Karnezos et al. (figures 1 to 18) specifically figure 3 show an assembly of packaged microelectronic devices, comprising: a support member **32**; a first packaged microelectronic device having a first microelectronic die **334** generally encased in a first encapsulant **33** and connected to the support member with a plurality of solder balls **36**; and a second packaged microelectronic device having a second microelectronic die generally encased in a second encapsulant **333** and connected to the support member with a plurality of elongated connection members **338** extending from the second packaged microelectronic device around at least part of the first packaged microelectronic device and attached directly to the support member.

64. The assembly of claim 65, Karnezos et al. show wherein the first packaged microelectronic device includes a first surface facing toward the support member, a second surface facing away from the support member and toward the second packaged

microelectronic device, and a plurality of third surfaces between the first and second surfaces, further wherein the elongated connection members **338** are positioned adjacent to the third surfaces of the first packaged microelectronic device.

66. The assembly of claim 65, Karnezos et al. show wherein the second package microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.

67. The assembly of claim 65, Karnezos et al. show wherein the support member includes support member circuitry, and further wherein all the elongated connection members **331,31,338** of the second microelectronic device are attached directly to the support member circuitry.

68. Karnezos et al. (figures 1 to 18) specifically figure 3 show an assembly of packaged microelectronic devices, comprising: a support member **32** having support member circuitry; a first packaged microelectronic device **34** electrically coupled directly to the support member circuitry; and a second packaged microelectronic device **334** electrically coupled directly to the support member circuitry without any direct electrical connections **338** to the first packaged microelectronic device, the first packaged microelectronic device being positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device not being fixed attached to the first packaged microelectronic device.

69. The assembly of claim 68, Karnezos et al. further comprising an elongated conductive connecting member **331,31,338** connected between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.

70. The assembly of claim 68, Karnezos et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

71. The assembly of claim 68, Karnezos et al. show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.
72. The assembly of claim 68, Karnezos et al. show wherein the first packaged microelectronic device is electrically coupled to the second packaged microelectronic device via the support member circuitry.
73. Karnezos et al. (figures 1 to 18) specifically figure 2 show an assembly of packaged microelectronic devices, comprising: a support member **12** having support member circuitry; a first packaged microelectronic device **(shown as 10 in figure 1A)** electrically coupled directly to the support member circuitry; and a second packaged microelectronic device **(shown as 11 in figure 1B)** connected directly to the support member with the first packaged microelectronic device being positioned between the support member and the second packaged microelectronic device, the second packaged microelectronic device not being fixedly attached to the first packaged microelectronic device.
74. The assembly of claim 73, Karnezos et al. show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the first and second packaged microelectronic devices.
76. The assembly of claim 73, Karnezos et al. show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second' edge of the first packaged microelectronic device.
77. The assembly of claim 73, Karnezos et al. show wherein the second packaged microelectronic device has a plurality of conductive members **223,28,121** electrically coupled to the microelectronic substrate and extending away from an encapsulant of the second microelectronic device, further wherein all the conductive members extending away from an encapsulant of the second microelectronic device are attached directly between the second packaged microelectronic device and the support member circuitry.

DOCUMENT-IDENTIFIER: US 20040119152 A1

Summary of Invention Paragraph - BSTX (42):
[0042] In another aspect the invention features a multi-package module having stacked first ("bottom") and second ("top") packages, the bottom package being a flip-chip BGA package having a flip-chip in a "die-up" configuration and the top package being an inverted LGA package, in which the top substrate and the bottom package are interconnected by wire bonding. In some embodiments the top package is a stacked die package; in some embodiments the adjacent stacked die in the stacked die package can be separated by spacers. In some embodiments the die on the BGA package is at least partially enclosed within an electrical shield (a "can" or "cage) affixed to the under surface of the BGA substrate. In some embodiments the bottom package substrate includes an embedded ground plane, the ground plane being configured to serve also for heat dissipation and as an electrical shield. In some embodiments a plurality of inverted second ("top") packages is affixed over a plurality of die attach regions on the upper surface of the first ("bottom") package substrate.

Response

Applicant's arguments filed 1/3/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,777,723,737,734,738,778,779,772,666,673, 668,687,678	8/31/04 3/29/05
Other Documentation: foreign patents and literature in 257/686,685,777,723,737,734,738,778,779,772,666,673, 668,687,678	8/31/04 3/29/05
Electronic data base(s): U.S. Patents EAST	8/31/04 3/29/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
3/29/05

Primary Patent Examiner
Alexander O. Williams